Abstract-- This paper proposes a novel UPFC based on 3-level half-bridge modules, isolated through single-phase multi-winding transformers. The dynamic performance of the proposed system was analyzed by simulations with EMTDC, assuming that the UPFC is connected to the 138-kV transmission line of a one-machine-infinite-bus power system. The proposed system can be directly connected to the transmission line without series injection transformers. It has flexibility in expanding the operation voltage by increasing the number of 3-level half-bridge modules.

Index Terms-- STATCOM (Static Synchronous Compensator), SSSC (Static Synchronous Series Compensator), UPFC (Unified Power Flow Controller), GTO (Gate Turn-Off thyristor), PWM (Pulse Width Modulation), PAM (Pulse Amplitude Modulation)

I. INTRODUCTION

UPFC, based on GTO voltage source inverters, was proposed as the most promising FACTS device to improve the dynamic performance of power transmission system. The dc link voltage of presently developed UPFC is much lower than the operation voltage of power transmission system [1]. This is due to the limit of high power semiconductor technology. The maximum sustain voltage of commercially available GTO is about 6000V.

A technique called series connection of GTO’s was developed to increase the dc link voltage of UPFC. However, still there is restriction in maximum allowable number of units. So, step-down transformers are normally used for properly matching the inverter operation voltage with the transmission voltage [2]. Multi-level inverter was proposed to increase the system operation voltage avoiding series connection of switching devices [3]. But the multi-level inverter has complexity in forming the output voltage and requires many back-connection diodes.

In order to complement this weak point, multi-bridge inverter composed of five H-bridge modules for each phase was proposed by Peng for STATCOM application [4,5]. The system operation was verified through experimental works with a scaled model.

The authors proposed two configurations of SSSC composed of H-bridge modules and 3-level H-bridge modules [6,7]. This system can operate without series injection transformers and has flexibility in expanding the operation voltage by means of adding the number of modules.

This paper proposes a novel UPFC based on 3-level half-bridge modules, isolated through single-phase multi-winding transformers. The operation of the proposed system was verified through simulations with EMTDC. The proposed system can be directly connected to the transmission line without series injection transformers.

II. UPFC

UPFC has two 3-level inverters connected in parallel through a common dc link capacitor as shown in Fig. 1. In configuration UPFC can be considered as a compound system of STATCOM and SSSC sharing a common dc link capacitor. However, UPFC has direct control capability of the real and reactive powers through transmission line. The shunt inverter has two functions. One function is to supply the real power required at the series inverter through the dc link capacitor, which maintains the dc link voltage constant to minimize the voltage variation of series inverter output. Another function is to improve the voltage stability at the connection point by regulating the reactive current.

The function of series inverter is to control the real and reactive powers independently by means of injecting an ac voltage with arbitrary magnitude and phase with the dc link voltage. The frequency of injection voltage is the same as that of the transmission system and its phase angle is determined by the inverter phase angle \( \alpha_{pq} \). The inverter phase angle can be adjusted within the range of \( 0 < \alpha_{pq} < 2\pi \). The magnitude of

![Fig. 1. System configuration of UPFC](image-url)
injection voltage $V_{pq}$ can be adjusted by changing the level of dc link voltage with the shunt inverter and by changing the conduction angle of series inverter. The computed injection voltage $V_{pq}$ is added to the terminal voltage $V$ and becomes $V + V_{pq}$.

III. PROPOSING UPFC

The 3-level inverter of commercially available UPFC [1] consists of several modules in parallel and operates in PAM pattern to eliminate the low order harmonics. Each module consists of twelve GTO switches and each switch is composed of several series-connected GTO’s to increase the operation voltage.

This paper proposes a novel UPFC based on several pairs of 3-level half-bridge modules per phase as shown in Fig. 2. Each pair has two 3-level half-bridge modules connected in parallel through a common dc link capacitor. One 3-level half-bridge module in shunt part is connected in series through single-phase multi-winding transformer for isolation purpose. The other 3-level half-bridge is directly inserted in the transmission line.

For the purpose of simulation convenience, the shunt and series parts are assumed to be composed of three 3-level half-bridge modules per phase as shown in Fig. 3(a) and 3(b). The output voltage of one module and switching pattern can be explained in Fig. 3(c).

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>SWITCHING PATTERN OF MULTI-BRIDGE INVERT</th>
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<tr>
<td>V1A</td>
<td>Switching State</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>S1, S2 : on and S3, S4 : off</td>
</tr>
<tr>
<td>0</td>
<td>S2, S3 : on and S1, S4 : off</td>
</tr>
<tr>
<td>$-V_{dc}$</td>
<td>S3, S4 : on and S1, S2 : off</td>
</tr>
</tbody>
</table>

The output of each module has three states $+V_{dc}$, 0, $-V_{dc}$ depending on states of switch S1-S4. Table I shows relationship between output voltage and switching state. By adjusting duration time, the output voltage can be adjusted.

Fig. 4 shows a principle of gate-pulse generation for PWM scheme. Fig. 4(a) shows two carrier signals and the reference signal to generate the gate pulses for inverter module INV1. The frequency of carrier T1, T2 is 480[Hz]. Each of two carriers has 180° phase shift with each other. Carriers to generate gate pulses for other inverter module has 120° phase shift with each other. The reference signal $V_{ref}$ has maximum value of 0.9 in per unit and has a sinusoidal waveform of 60Hz. Fig. 4(b) shows how to generate the gate pulses using the reference and carrier signals. Carrier T1 and T2 are used as the input to generate gate pulses for inverter module.

Fig. 5 shows the output voltage waveforms of each inverter modules, V1, V2, V3, and the total output voltage of three inverter groups, where the dc voltage $V_{dc}$ is 1.0 per unit. As explained before, the carrier shown in Fig. 4(a) is used to generate gate pulses for building up output voltage V1. Two sets of carriers with 180° phase shift from each other are needed to generate gate pulses for building up output voltage V2 and V3. These sets of carriers have 120° phase shift with...
each other. Since each carrier has a frequency of 480[Hz] and there are six carriers, total output voltage VA has an equivalent switching effect of 3[kHz]. THD of output voltage VA is about 3% and spectra of harmonics are located around 3kHz. Therefore, these harmonics can be easily filtered out.

Fig. 6 shows the configuration of voltage balance controller for the dc capacitor. Separate control was considered for each phase. There are three controllers in the proposed UPFC. The controller measures the voltage at the common connection point of shunt inverter. This value is used to calculate the phase-lock angle $\theta$ by passing through the phase-lock loop. This value is adjusted by means of adding $2\pi/3$ or $4\pi/3$ for each phase.

The total dc link voltage is obtained by means of measuring each capacitor voltage with an isolated sensor and adding together. This voltage is used to obtain the average voltage of each capacitor by means of dividing by three. The average voltage is compared with the measured voltage of each capacitor and the error is passed through the error amplifier and the limiter to obtain the phase-angle deviation $\Delta \alpha$. The phase-angle deviation $\Delta \alpha$ is added to the phase-angle $\alpha$ and the phase-lock angle $\theta$. The total phase-angles are sent to the sine wave generator to obtain the reference signals Ref1, Ref2, Ref3, which have the phase deviation. There are two same types of controller to provide the reference signals to the gates of H-bridge in other two phases.

IV. EMTDC SIMULATION

In order to analyze the operation of proposed UPFC based on multi-bridge inverter, computer simulations with EMTDC were performed. The power system is represented by one-machine-infinite-bus pattern. The transmission line is modeled with a reactor considering only lumped line reactance. The circuit parameters used in the simulation are shown in Table II.

<table>
<thead>
<tr>
<th>TABLE II</th>
<th>SIMULATION PARAMETER</th>
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<tbody>
<tr>
<td>Base voltage</td>
<td>112.676[kV]</td>
</tr>
<tr>
<td>Base current</td>
<td>946 [A]</td>
</tr>
<tr>
<td>Rate voltage</td>
<td>138 [kV]</td>
</tr>
<tr>
<td>Power angle</td>
<td>20°</td>
</tr>
</tbody>
</table>
Fig. 7 shows a detail configuration of the UPFC controller used in the simulation. Fig. 7(a) shows a control block diagram for the series inverter and Fig. 7(b) for the shunt inverter in automatic power flow control mode. The automatic power flow control is achieved by means of a vector control scheme that regulates the transmission line current using a synchronous frame, in which the control quantities appear as dc signals in the steady state. The appropriate reactive and real current components, \(i_q^*\) and \(i_p^*\), are determined for a desired \(P_{\text{ref}}\) and \(Q_{\text{ref}}\). These are compared with the measured line currents, \(i_q\) and \(i_p\), and used to drive the magnitude and angle of the series inverter voltage, \(V_{pq}\) and \(\rho\), respectively. In the control scheme for the shunt inverter, the magnitude of the output voltage is directly proportional to the dc voltage and only its angle is controllable. The outer voltage loop regulates the ac bus voltage and also controls the dc capacitor voltage. This outer loop changes the phase angle \(\alpha\) of the inverter voltage with respect to the ac bus voltage until the dc capacitor voltage reached the value necessary to achieve the reactive compensation demanded.

The scenario considered in this simulation is shown in Table III. It is assumed that the maximum simulation time is 5.5 second. The reference value of \(P\), which is initially 250 MW, suddenly changes at 1.5, 2.5, 3.5, and 4.5 second as shown in the Table II. The reference value of \(Q\), which is initially 0 MVar, suddenly changes at 2.5 second as shown in Table III.

Fig. 8 shows the simulation results for the performance analysis of the proposed UPFC system with EMTDC. Fig. 8(a) and 8(b) shows the tracking capability of the proposed UPFC with respect to the step-changes of \(P\) and \(Q\) reference values. It is clear that the series inverter injects a proper voltage into the transmission line to make the \(P\) and \(Q\) through the transmission line follow the reference values of \(P_{\text{ref}}\) and \(Q_{\text{ref}}\). Fig. 8(c) shows that the shunt inverter maintains the bus voltage constant by means of STATCOM operation. Fig. 8(d) shows the variation of each dc link capacitor in phase A. Although there is dispersion due to the PWM switching, it is known that the voltage of each capacitor is balanced evenly.

Fig. 8(e) shows the voltage variation at each dc capacitor of one phase, when it is in unbalanced condition. It is assumed that each capacitor voltage, which is balanced initially, falls sudden into the unbalanced state at 1.4 sec. The voltage-balancing controller is activated at 1.8 sec. This result confirms that the controller shown in Fig. 6 operates perfectly to make the dc link voltage balanced.
There are twelve pairs of 3-level half-bridge modules for each phase in the proposed UPFC. The maximum injection voltage in series part is assumed 50% of the operation voltage (phase voltage of 40kV). The turn-ratio of primary to each secondary winding in the single-phase multi-winding transformer is designed to be 24:1. The RMS voltage to be handled by each 3-level half-bridge is 3.33kV, which is tolerable because each 3-level half-bridge takes over this voltage with two GTO’s of 4kV DC off-state voltage with enough safety.

Fig. 9 shows the conceptual diagram of the proposed UPFC system including the simple power system. The proposed UPFC has twelve pairs of 3-level half-bridge module for each phase. There are thirty-six pairs of 3-level half-bridge module, in which each pair of 3-level half-bridge has eight GTO’s. Therefore, two hundred eighty-eight GTO’s in the proposed UPFC are required in total.

VI. Conclusion

This paper proposes a novel UPFC based on 3-level half-bridge modules, isolated through single-phase multi-winding transformers. The dynamic performance of proposed system was analyzed by simulation with EMTDC, assuming that the UPFC is connected with the 138-kV transmission line of one-machine-infinite-bus power system. The proposed system can be directly connected to the transmission line without series injection transformers. It has flexibility in expanding the operation voltage by increasing the number of 3-level half-bridge modules.

The contribution of this paper is to propose a novel structure of UPFC to be connected in the transmission line directly without series injection transformer. The series transformer is a critical item in UPFC because it should have low saturation effect and leakage impedance. The developed simulation model could be used to obtain design data for actual hardware system.

V. System Realization

The system realization aims at the development of a practical system that can be built with commercially available and reliable components. A commercially available high-power GTO, Mitsubishi FG6000AU-120D, was considered for the building block of 3-level half-bridge. It has the rating of 6kV peak off-state voltage (4.8kV DC off-state voltage) and 6kA controllable on-state current (1.5kA average on-state current). In order to guarantee enough safety, 4kV DC off-state voltage and 1.25kA average on-state current were considered for the system design.

It is assumed that the proposed UPFC has 138kV of nominal operating voltage and 150MVA of power rating.
VII. REFERENCE


VIII. BIOGRAPHIES

B. Han(S’91-M’92-SM’00) received the B. S. degree in electrical engineering from the Seoul National University, Korea in 1976, and the M. S. and Ph.D. degree from Arizona State University in 1988 and 1992, respectively.

He was with Westinghouse Electric Corporation as a senior research engineer in the Science & Technology Center. Currently he is a professor in the Department of Electrical Engineering at Myongji University, Korea. His research interests include the high-power power electronics and FACTS.

Paolo Mattavelli received his Dr. degree with honors in electrical engineering from the University of Padova, Italy, in 1992. In 1995 he received his Ph.D. studies in electrical engineering in the same university. From 1995 to 2001, he was a researcher at the University of Padova. In 2001 he joined the Department of Electrical, Mechanical and Management Engineering (DIEGM) of the University of Udine, where he has been an Associate Professor since 2002. His major field of interest include analysis, modeling and control of power converters, digital control techniques for power electronic circuits, active power filters and high power converters.