Autotuning of Digitally Controlled Buck Converters based on Relay Feedback

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Abstract— This paper proposes a simple autotuning technique for digitally controlled dc-dc synchronous buck converters. The proposed approach is based on the relay feedback method and introduces perturbations on the output voltage during converter soft-start. By using an iterative procedure, the tuning of PID parameters is obtained directly by including the controller in the relay feedback and by adjusting the controller parameters based on the specified phase margin and control loop bandwidth. A nice property of the proposed solution is that output voltage perturbations are introduced while maintaining the closed-loop control of the digitally controlled converters. The proposed algorithm is simple, requires small tuning times and it is compliant with the cost/complexity constraint of integrated digital ICs. Experimental investigation confirm the effectiveness of the proposed solution.

I. INTRODUCTION

Integrated digital controllers for Switch-Mode Power Supplies (SMPS) are gaining growing interest, since it has been shown the feasibility of digital controller ICs specifically developed for high-frequency switching converters [1-4]. One very interesting potential benefit is the use of autotuning of controller parameters, so that the dynamic response can be set at the software level, independently of output capacitor filters, component variations and aging. In order to be an interesting solution, however, the autotuning process should satisfy two important requirements: 1) it should not affect converter operation under nominal condition and 2) it should be based on a simple and robust algorithm whose complexity does not require a significant increase of the silicon area of the IC controller. The first issue may be handled by performing controller autotuning during converter soft-start, where there are some degree of freedom for the introduction of output voltage perturbations. The second issue is much more challenging and requires the development of “ad-hoc” autotuning techniques specifically tailored for integrated digitally-controlled converters.

Several auto-tuning techniques for classical regulator structures (such as Proportional-Integral-Derivative (PID)) have been widely discussed in literature [5-9]. The great effort was motivated by the fact that PID regulators are widely accepted in industrial applications and by the fact that the applications of microcontrollers and DSPs have been rapidly increased in power electronics/drives applications, mainly in the medium/high power range. Note, however, that most of the existing solutions are too complex for small-power dc-dc converters with integrated digital controllers due to the cost/complexity constraints existing in these applications. Some results of non-parametric methods for the on-line assessment of system dynamics in dc-dc converters are discussed in [10,11]; the methods reported in [10,11] are very interesting for converter transfer functions identifications, but they requires open-loop operation during the identification process and complex signal processing.

This paper proposes a simple autotuning method for voltage-mode synchronous buck converters, applied as Point of Load converters (PoLs), by using the relay feedback [5]. By means of the relay control, small oscillations on the output voltage are generated during converter soft-start. Based on the measurements of the frequency and amplitude of the oscillations, the gain and phase of the converter transfer function at the oscillation frequencies are derived. Instead of estimating the converter transfer function at different frequencies, the paper proposes an iterative procedure, where the tuning of PID parameters is obtained directly by including the controller in the relay feedback and by adjusting the controller parameters based on the specified system phase margin and loop bandwidth. The proposed algorithm is simple and it requires small tuning times. Simulation and experimental results on a synchronous buck converter confirm the effectiveness and limitations of the proposed solutions.

II. BASICS OF AUTOTUNING USING RELAY FEEDBACK

The basic principle of relay feedback method can be explained following Fig. 1. The converter transfer function, which is going to be controlled, denoted with $G(s)$, is regulated firstly using a relay (see Fig. 1a). Thus, an oscillation on signal $y$ with period $T_0$ (or angular frequency $\omega_0$) and amplitude $a$ is generated (see Fig. 1b). The oscillation waveform is almost sinusoidal assuming that the low-pass filter action of $G(s)$ filters the higher harmonics generated by the relay. The condition for the oscillation to be maintained is the following

$$N(a) \cdot G(j\omega_0) = -1$$  \hspace{1cm} (1)
where \( N(a) \) is the relay transfer function modeled using the describing function method, i.e.:

\[
N(a) = \frac{4D_r}{\pi a}
\]

and \( D_r \) is the amplitude of the square-wave generated by the relay. Condition (1) is also represented in the Nyquist diagram of Fig. 1c where \( G(j\omega) \) intersects \(-1/N(a)\) and it clearly shows that the systems oscillates when the phase of \( G(j\omega) \) is \(-180^\circ\). Practical implementation of the scheme of Fig. 1 usually requires the introduction of an hysteresis function in the relay block. In this case, the describing function of the relay is

\[
N(a) = \frac{4D_r}{\pi \left( \sqrt{a^2 - \varepsilon^2} + j\varepsilon \right)}
\]

where \( \varepsilon \) is the hysteresis width. This function can be represented as a straight line parallel to the real axis, in the complex plane. The contribution of the imaginary part in (3) is usually very small, so that the system still oscillates when the phase of \( G(j\omega) \) is very close to \(-180^\circ\). Controller autotuning is usually obtained by measuring the oscillation period \( T_u \) and amplitude \( a \) and then by deriving the PID coefficients using Ziegler-Nichols formulas [5].

This basic approach is, however, not very suitable for dc-dc converters since Ziegler-Nichols formulas are quite conservative, they do not use the a-priori information on the dynamic structure of \( G(s) \), usually available in dc-dc converters, and thus they do not usually yield to an optimal dynamic response. The Ziegler-Nichols method may be used as a pre-tuner, but then manual tuning is needed to obtain dynamic performances satisfactory for high-performance dc-dc converters.

III. AUTOTUNING OF PID PARAMETERS FOR BUCK CONVERTERS

In voltage-mode synchronous buck converter, the transfer function between the duty-cycle and the output voltage is simply given by the second order output filter, i.e.:

\[
G(s) = \frac{V_o(s)}{\delta(s)} = \frac{V_{in} + \frac{1 + s\tau_{esr}}{\omega_o}}{1 + \frac{2\xi}{\omega_o}s + \frac{s^2}{\omega_o^2}}
\]

where \( \omega_o = \sqrt{\frac{1}{LC}} \), \( \xi = (R_{dwell} + R_{esr} + R_{esr})/Z_o \), \( Z_o = \sqrt{L/C} \) (see Fig. 2). The equivalent series resistance \( R_{esr} \) is neglected in the case of ceramic capacitors, while it plays an important role in the case of electrolytic capacitors. The case of non-negligible ESR is usually less critical from the PID autotuning point of view, since the derivative action on the high-frequency range is not needed and a simpler PI (Proportional-Integral) controller structure is sufficient for the voltage loop regulator. For the purpose of explanation, the general case of PID control is considered. In the case of electrolytic capacitors, the autotuning technique sets the derivative gain to a negligible value.

The PID regulator structure can be expressed as

\[
PID(z) = \frac{K_I}{1-z^{-1}} + K_P + K_D(1 - z^{-1}) = \frac{K_{PID}(1-b_{z2}z^{-1})}{1-b_{z1}z^{-1}}
\]

where the PID transfer function has been decomposed so as to highlight the integral term \((1-z^{-1})\) and two zeros, having time constants \(\tau_{z1}\) and \(\tau_{z2}\).

The most general approach for controller autotuning may be divided in three phases. In the first phase (denoted Phase A), the system is forced to oscillate at the resonant frequency \(\omega_o\) and the first zero \((\tau_{z1})\) is set at the resonant frequency. In the second phase (denoted Phase B), an iterative procedure is used to tune the second zero \((\tau_{z2})\) so as to satisfy the specification on the desired phase margin and in the third and last phase (denoted Phase C) the gain \(K_{PID}\) of the PID control is tuned so as to impose the desired bandwidth. A set of simplifications of this general
procedure is possible, if a priori knowledge of some converter parameters is available.

A. Resonant frequency identification and tuning of $\tau_1$

In the first phase, the system is forced to oscillate at the resonant frequency $\omega_0$. As shown in Fig. 2, this is simply obtained by adding an integral term in the feedback loop so that transfer function $G(s)$ and the integrator gives -180° exactly at the resonance angular frequency $\omega_0$. Taking into account the possible calculation delay of the digital controller and the Zero-Order-Hold (ZOH) sampling of the converter transfer functions, the oscillation is usually just before the resonant frequency.

Since the system is excited closed to the resonant angular frequency $\omega_0$, in some applications it may be important to add an active damping of the LC filter so as to limit the amplitude of the oscillations on the output voltage. This may be needed in the case of lightly damped LC output filter. Active damping is simply obtained introducing a small derivative action, as reported in Fig. 2. Since the goal is only to avoid undesired amplification at the resonant frequency, a rough estimation of the damping coefficient $k_s$ is sufficient for wide parameter variations on the LC filter.

Following Fig. 2, the output of phase A is the estimation of LC angular resonance frequency $\omega_0$ and the measurement of the transfer function (4) at the resonance frequency. Based on this estimation, the zero at $\tau_1$ has been set to be at the resonance frequency $\omega_0$ (i.e. $\tau_1=1/\omega_0$). If the zero due to the output capacitor is known, then it is possible to directly complete the PID (or PI) tuning. For example, in the case of ceramic capacitor it is possible to set the second zero $\tau_2$ at the same frequency (i.e. $\tau_2=1/\omega_0$) and then tune the gain of the PID according to the specified control loop bandwidth $\omega^*$. Such simplifications, which may be very useful in some specific applications, are not here considered. As a general approach, we preferred to add a second phase of tuning (in Fig. 2 denoted Phase B) in order to optimize system response and to propose a technique which is independent of output capacitor behavior. Moreover, the placement of both zeros $\tau_1$ and $\tau_2$ at $1/\omega_0$ may be conservative in the case the LC resonant angular frequency $\omega_0$ is much lower than the desired control loop bandwidth $\omega^*$ or it may give small phase margin in the case $\omega_0$ is very close to $\omega^*$. In this latter case, which is, however, not very common, the zero $\tau_1$ should be placed below $\omega_0$ so as to ensure the leading action at the desired bandwidth $\omega^*$.

B. Iterative tuning of $\tau_2$ based on phase margin specification

During phase B, the zero $\tau_2$ is iteratively tuned so as to give the specified oscillation frequency $\omega_{osc}$. Since the system oscillates when the loop gain is -180°, an additional low-pass filter $F(z)$ (see Fig. 2) is needed in order to force the desired phase margin $m^*$. In fact, when the system oscillates at angular frequency $\omega_{osc}$ due to the relay feedback, we have

$$\arg(F(e^{j\omega_{osc}T_{sw}})) + \arg(PD(e^{j\omega_{osc}T_{sw}})) + \arg(PI(e^{j\omega_{osc}T_{sw}})) + \arg(G_d(e^{j\omega_{osc}T_{sw}})) = -\pi$$

where $G_d(z)$ is the zero-holder-hold sampling of $G(s)$. Thus, when $\omega_{osc} = \omega^*$, the closed loop system has the desired
phase margin $m_\phi$ since (6) can be rearranged as:

$$\arg(PD(e^{i\omega osc T_{sw}})) + \arg(PI(e^{i\omega osc T_{sw}})) + \arg(G_1(e^{i\omega osc T_{sw}})) = -\pi + m_\phi$$  \hspace{1cm} (7)

If $\omega_{osc} > \omega^*$, the lagging phase of $F(z)$ is greater than $m_\phi$ (i.e., $\arg(F(e^{i\omega_{osc} T_{sw}})) < -m_\phi$) and the system phase margin is greater than the specified value $m_\phi$ (i.e., the lagging phase of $PI(z)$ is lower than the correct value). Thus, the value of zero $\tau_{z2}$ has to be reduced. Conversely, if $\omega_{osc} < \omega^*$ the lagging phase of $F(z)$ is lower than $m_\phi$ (i.e., $\arg(F(e^{i\omega_{osc} T_{sw}})) > -m_\phi$) and the system phase margin is lower than the specified value $m_\phi$, and thus, the value of zero $\tau_{z2}$ has to be increased. This iterative procedure, using the bisection method, is a simple but effective way to find the correct solution. We found that just a few iterations (3-4) are needed to obtain a good approximation of the correct value.

C. Tuning of controller gain based on specified bandwidth

Once the iteration process is over, the gain of the PID ($K_{PID}$) is calculated from the attenuation introduced by the low-pass filter $F(z)$ and the gain calculated from the describing function of relay, i.e.:

$$K_{PID} = \frac{4 D_r(k)}{\pi V_{osc}} |F(e^{j\omega_{osc} T_{sw}})|$$  \hspace{1cm} (8)

where $V_{osc}(k)$ is the amplitude of the oscillations during the last iteration, evaluated as:

$$V_{osc}(k) = \frac{\pi}{2 N_{samp}} \sum_{h=1}^{N_{samp}} [v_o(h) - v_o^{ref}]$$  \hspace{1cm} (9)

where $N_{samp}$ is the number of samples over the measured interval.

IV. SIMULATION RESULTS

The proposed solution has been verified using simulation tools on a synchronous buck dc-dc converters having the following parameters: $V_{in}=5 \text{ V}$, $V_o=1.5 \text{ V}$, $L=3 \mu\text{H}$, $C=600+1000\mu\text{F}$, $f_{sw}=200 \text{ kHz}$. In the simulation model, the digital control has been implemented with a sampling frequency equal to the switching frequency and with negligible calculation delay.

The proposed autotuning is performed during converter soft-start. More precisely, the output voltage is kept below the nominal value during the autotuning procedure. For example, in this paper we have set that the autotuning is performed at the 80% of the nominal voltage. The first step is to achieve 80% of output nominal voltage with a specified ramp: to ensure system stability, in this phase the voltage loop is closed with the relay and integrator inserted. The slope of the output voltage ramp can be adjusted varying the relay amplitude and the integral constant. When the output voltage reaches the 80% of the nominal value, then the autotuning procedure is started. Details of the autotuning method are reported in Fig. 3, which highlights the phases A and B and the iteration process during phase B. During Phase A, because the loop gain is unknown, the first $D_r$ amplitude must be chosen small enough to avoid overvoltages and successively adjusted according to the following algorithm:

$$D_r(k) = \frac{V_{osc_{max}}}{V_{osc}(k-1)} \cdot D_r(k-1)$$  \hspace{1cm} (10)

where $V_{osc_{max}}$ is the desired oscillation amplitude, $V_{osc}(k-1)$ is the oscillation amplitude and $D_r(k-1)$ is relay amplitude both at instant $k-1$. Very small oscillations amplitudes may compromise the correctness of frequency estimation because 2nd order effects and noise disturbances. Moreover, stable measurement of the oscillation amplitude requires an observation interval equal to several oscillation periods (typically 4-6), both for transient adjustment and noise rejection. At the end of phase A, $\tau_{z2}$ is set at $1/\omega_{osc}$.

For each iteration during phase B, the amplitude of $D_r$ needs to be adjusted as described in phase A. Instead of starting from a very small value, at each change of $\tau_{z2}$, it is possible to estimate the initial value of $D_r$ that ensures the desired oscillations amplitude as follows:

$$D_r(k) = D_r(k-1) \cdot \frac{\tau_{z2}(k-1)}{\tau_{z2}(k)} \cdot \frac{f_c}{f_{osc}(k-1)}$$  \hspace{1cm} (11)

This algorithm is based on the assumption that the PID regulator has -20 dB/dec at the cross-over frequency and that the system oscillates near the cross-over frequency at the next step. The purpose of this algorithm is to compensate the change of loop gain when the 2nd zero is moving. However, we found that an alternative and much simpler solution is to halve $D_r$ amplitude at each change of $\tau_{z2}$ and then to apply algorithm (10).

In Fig. 4 it is shown the detail of bode plot at cross-over

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**Fig. 3** – Converter soft-start with the proposed auto-tuning procedure
frequency of the system loop at each iteration when \( \tau_{z2} \) is tuned (phase B): this figure highlights the change of oscillating frequency at every change of \( \tau_{z2} \). The loop gain plotted is calculated taking into account the gain introduced by the describing function of the relay. The autotuning has been performed with a desired crossover frequency equal to 16.6 kHz and phase margin equal to 45°.

Fig. 5 and 6 report the converter dynamic behavior following a load step change with the output capacitor equal to 1000 \( \mu F \) and 600 \( \mu F \), respectively. Note that, in spite of using the double of the output capacitor, the time response to load changes remains almost the same and the dynamic behavior is well damped, verifying the effectiveness of the proposed solution.

Fig. 8 shows the comparison between final values of controller parameters (\( \tau_{z1}, \tau_{z2}, K_{PID} \)) for the case of tantalum capacitors and ceramic capacitors. In the case of tantalum capacitors, due to the presence of the zero \( \tau_{esr} \) within the control bandwidth (placed at 12 kHz in our case), the 2\(^{nd} \) zero of the PID regulator is placed at high frequencies and, thus, it can be neglected.

### Table I– Autotuning results with different output capacitors

<table>
<thead>
<tr>
<th></th>
<th>( f_{z1} )</th>
<th>( f_{z2} )</th>
<th>( K_{PID} )</th>
<th>( m_\phi )</th>
<th>( f_c )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ceramic capacitors</td>
<td>3.74 kHz</td>
<td>3.83 kHz</td>
<td>0.0918</td>
<td>45°</td>
<td>16.6 kHz</td>
</tr>
<tr>
<td>Tantalum capacitors</td>
<td>4.16 kHz</td>
<td>29 kHz</td>
<td>0.214</td>
<td>60°</td>
<td>16.6 kHz</td>
</tr>
</tbody>
</table>

Fig. 5 – Load step change (\( I_o = 0 \text{ A} \rightarrow 5 \text{ A} \)) after autotuning with ceramic capacitor equal to 1000 \( \mu F \).

V. EXPERIMENTAL RESULTS

The proposed autotuning algorithm has been tested on a synchronous buck dc-dc converter having the following parameters: \( V_{in}=5 \text{ V} \), \( V_o=1.5 \text{ V} \), \( L=3 \mu H \), \( C=600-1000 \mu F \) for ceramic capacitors and \( C=660-1320 \mu F \) for tantalum capacitors, \( f_{sw}=200 \text{ kHz} \). The digital control has been implemented in an FPGA (the EP1C20 device, a member of Cyclone family by Altera). Due to the ADC conversion time, the digital control is characterized by a delay between sampling and DPWM update equal to half-switching period delay; thus, the achievable dynamic performances has been limited to 1/15 of the switching frequency.

Fig. 7 shows the output voltage during autotuning phase with ceramic capacitors equal to 1000\( \mu F \) imposing a loop bandwidth of \( f_{sw}/15 \) and phase margin 30°. As a results of the autotuning process, \( f_{z1}=2.85 \text{ kHz} \) and \( f_{z2}=5.6 \text{ kHz} \). The converter dynamic behavior following a step load current is reported in Fig. 8. In order to verify the effectiveness of the proposed autotuning procedure, the output capacitor value has been decreased from 1000\( \mu F \) to 600\( \mu F \). The autotuning process have set the following control parameters: \( f_{z1}=3.7 \text{ kHz} \) and \( f_{z2}=3.36 \text{ kHz} \). As reported in Fig. 9, the dynamic behavior is almost unchanged, as theoretically foreseen. The voltage drop is, of course, bigger due to the decreased capacitor value. Note that the increased voltage drop is not linearly dependant on the inverse of the output capacitor due to the control delay effect.
The same procedure has been applied to tantalum capacitors imposing a loop bandwidth of $f_{sw}/15$ and phase margin $60^\circ$. For $C=1320 \ \mu F$, the autotuning procedure gives $f_{z1}=2.7 \ \text{kHz}$ and $f_{z2}=13.4 \ \text{kHz}$. For $C=660 \ \mu F$, the autotuning procedure gives $f_{z1}=4.0 \ \text{kHz}$ and $f_{z2}=13 \ \text{kHz}$. In this case, the derivative contribution of the PID regulator is used for the compensation of control delay. The converter dynamic behavior following a load step up is reported in Figs. 10-11 and they confirm the effectiveness of the proposed method.

VI. CONCLUSIONS

This paper has proposed an autotuning technique for digitally controlled dc-dc synchronous buck converters based on the relay feedback. In the proposed solution, output voltage perturbations have been introduced during converter soft-start, while maintaining the closed loop operation of the converter. By using an iterative procedure, the tuning of PID parameters is obtained directly by including the controller in the relay feedback and by adjusting the controller parameters based on the specified phase margin and control loop bandwidth. Experimental results have verified the performance of the proposed solution.

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