Abstract—This paper investigates the application of a mixed synchronous/asynchronous digital controller to dc-dc boost converters. The digital control synchronously generates current and voltage ramps by using two low-resolution Digital-to-Analog Converters (DACs). Switch turn-on and turn-off are determined asynchronously by comparing converter state variables and the digitally generated current and voltage ramps. The control features high dynamic performance, frequency modulation during transients, no quantization effects, and low-complexity. In order to evaluate the dynamic performance and to compare the proposed solution with conventional analog peak current-mode control, a small signal model of the synchronous/asynchronous modulation is derived. Even if aimed to an integrated digital controller, experimental investigation has been performed using discrete components, implementing the digital control in a Field Programmable Gate Array (FPGA) using a hardware description language (VHDL). Simulation and experimental results on 100 W dc-dc boost converter confirm the proposed analysis and show that the proposed solution enables dynamic performance comparable to that of analog peak current-mode control.

I. INTRODUCTION

Integrated digital controllers for Switch-Mode Power Supplies (SMPS) are gaining growing interest, since when it has been shown the feasibility and advantages of digital controller ICs specifically developed for high-frequency switching converters [1-8]. Indeed, integrated digital controllers for SMPS potentially offer some interesting advantages compared to their analog counterparts, due to their immunity to component variations, ability to implement sophisticated control schemes and system diagnostics and, from the integrated design point of view, faster design process, ease of integration with other digital systems, and straightforward scaling with the advances in fabrication technologies. One of the main limiting factors for the use of IC digital controllers in SMPS is the achievement of performances comparable to those of analog controllers in presence of non-idealities such as control delays and quantization effects. Thus, one of the major needs in digital control for SMPS is the development of simple digital or mixed-signal control architectures with reduced silicon area requirements, which ensure dynamic performance comparable to analog controllers.

Most of the digital controllers developed up to now [1-8] are based on a conventional architecture where Analog-to-Digital Converters (ADCs) are used to digitalize the converter state variables and a digital control algorithm determines the duty-cycle, which drives the Digital Pulse Width Modulator (DPWM). In order to limit the complexity of the digital controller, low resolution ADCs and DPWM are usually needed [2], which unfortunately enhance undesirable quantization effects and limit cycle oscillations. For this reason, the development of alternative digital (or mixed-signal) control architectures, which overcome the limitations of conventional solutions, is a challenging future trend in SMPS control field. One effective solution in this direction has been proposed in [9] for Voltage Regulation Modules (VRM). The control architecture is based on DACs with low resolution and on a combination of current programming and variable frequency operation. However, investigation in [9] does not clearly address the dynamic properties especially with converters having right-half plane zeros in the transfer function between the duty-cycle and output voltage, such as the boost converters.

This paper proposes the investigation of mixed synchronous/asynchronous digital controller [9] to dc-dc boost converters. The digital control synchronously generates current and voltage ramps by using two low-resolution Digital-to-Analog Converters (DACs). Switch turn-on and turn-off are determined asynchronously by the comparison between converter state variables and the digitally generated current and voltage ramps. An interesting result of this paper is the verification that the combination of synchronous/asynchronous control enables high dynamic performances, practically comparable to those obtainable with conventional analog peak current-mode control. A small signal model of the proposed modulation has been derived and used for the analysis of the dynamic properties and for the derivation of controller design. Simulation and experimental results confirm the proposed analysis.
II. BASICS OF SYNCHRONOUS-ASYNCHRONOUS DIGITAL CONTROL

Fig. 1 shows the basic scheme of the synchronous-asynchronous digital control applied to dc-dc boost converters. We recall [9] that switch turn-on and turn-off are determined by the logic signal \( \text{Comp}_I\) and \( \text{Comp}_V\). When inductor or switch current exceeds the reference signal \( R_d(t)\) generated by DACI, the switch is turned off similarly to peak current-mode control. When the output voltage is lower than the reference signal \( R_d(t)\) generated by DACV, the switch is turned on. While the switch turn-on and turn-off is determined asynchronously by the comparator status, the digitally generated ramps are synchronous with system clock. Signal \( R_d(t)\) generated by DACI includes a peak current level \( i_{pk}(t)\) and a current ramp with negative slope (-\( s_I\)), which ensures the absence of sub-harmonic oscillations for duty-cycle greater than 0.5. Signal \( R_d(t)\) generated by DACV includes a constant reference voltage \( V_{ref}\), which is in practice generated outside the DAC in order to optimize DAC resolution, and a variable bottom level \( v_{os}(t)\) of the voltage ramp on which a voltage ramp with positive slope (\( s_V\)) is superimposed. Main control waveforms in steady-state conditions are reported in Fig. 2, where the DAC outputs are slightly filtered.

As any conventional digital control architecture, which requires some analog components for the ADC, the scheme of Fig. 1 includes some analog blocks (two low-resolution DACs and two comparators), which are however very simple, not accurate and require a small silicon area for its IC implementation. Thus, the digital control architecture is very effective from the IC point of view.

For the purpose of explanation, current and voltage slopes are approximated with constant values, \( s_I\) and \( s_V\), respectively. Moreover comparators and switch on/off propagation delays are here neglected. Under steady-state conditions, the average inductor current \( I_L\) and the average output voltage \( V_o\) are given by:

\[
I_L = I_{\text{pk}} - s_I \cdot D \cdot T_{\text{sw}} - V_{\text{in}} \cdot D \cdot \frac{T_{\text{sw}}}{2L} \quad (1)
\]

\[
V_o \geq V_{\text{ref}} - V_m + s_V \cdot T_{\text{sw}} \quad (2)
\]

where capital letters indicate steady-state values, \( T_{\text{sw}}\) is the steady-state switching period, \( D\) is the steady-state duty cycle and \( V_m = s_V \cdot T_{\text{sw}}^{ref}\), being \( T_{\text{sw}}^{ref}\) the reference switching period. Equation (2) indicates that steady-state output voltage is regulated by the switching period \( T_{\text{sw}}\). Instead, (1) indicates that switching period \( T_{\text{sw}}\) can be controlled by varying the peak current \( I_{\text{pk}}\), since \( I_L\) and \( D\) are constant for a given load condition.

In practice, the combination of DACV, \( \text{Comp}_V\) and the digital controller act as an equivalent ADC that converts the voltage error \( \varepsilon_{vo} = (V_o - V_{\text{ref}})\) into a switching period error

\[
\varepsilon_{sw} = (T_{sw} - T_{sw}^{ref}) \quad (3)
\]

The sampled error voltage \( \varepsilon_{sw}\) is then obtained by multiplying the switching period error by the voltage slope. Regulation of the switching period \( T_{sw}\) is performed by controlling the peak current \( I_{pk}\) with a Proportional-Integral (PI) control \( (reg_{if}(z))\) on the sampled voltage error \( \varepsilon_{sw}\).

In some instances, the bottom level of the voltage ramp may be kept constant (switches in position (a) in Fig. 1), i.e. \( v_{os}(t) = V_m\); this operating mode is denoted Case A. In other cases, \( v_{os}(t)\) is modulated in order to track the output voltage variations. This may be needed, for example, if the voltage slope \( s_V\) is very small so as to avoid converter saturation during transient conditions. A possible solution to control \( v_m\) is to impose a deadbeat regulation on the switching period \( T_{sw}\), as depicted in Fig. 3. Once the switching period is measured, the next voltage ramp amplitude is set so as to cancel the switching period error in the following switching cycle. Thus, looking at Fig. 3, a control algorithm is derived, based on sampled variables at instant \( k\), so as to impose

\[
v_m(k) = V_m + \Delta v_m(k) \quad (3)
\]

\[
\Delta v_m(k) = \Delta v_m(k-1) + s_v \left[ T_{sw}^{ref} - T_{sw}(k) \right]
\]

Equation (3) ensures that \( \Delta v_m(t)\) tracks output voltage error based on a predictive control on the switching period \( T_{sw}\); this
operating mode is denoted Case B. In order to understand the effect of (3) on the closed-loop control, the relation between the sampled output voltage error \( e_{vo} = e_{vo}(k) \) and the switching period \( t_{sw}(k) \) is derived. Looking at Fig. 3, we can write:

\[
v_m(k) - e_{vo}(k+1) = s_v t_{sw}(k)
\]

(4)

where \( e_{vo}(k) = V_{o}^{ref} - V_o(k) \). By rearranging (3) and (4), the switching period \( t_{sw}(k) \) can be expressed as:

\[
t_{sw}(k) = T_{sw}^{ref} + \frac{1}{s_v} \left[ e_{vo}(k+1) - e_{vo}(k) \right]
\]

(5)

Thus, for a given constant output voltage error \( e_{vo} \), the switching period error goes to zero in one sample delay, as expected by the predictive control. The main drawback is that (5) is a derivative action between the output voltage error \( e_{vo} \) and the switching period variation. Thus, if the input of regulator \( \text{regT}(z) \) is the switching period error \( \epsilon_{sw} \), a double integrator is required for ensuring zero steady-state error. In order to avoid more complex regulator structure respect to a conventional Proportional-Integral (PI) control, \( \Delta v_m(k) \) is used as the input of the regulator \( \text{regT}(z) \), as reported in Fig. 1 (switches in position (b)). In fact, rearranging (3) and (4), we have:

\[
\Delta v_m(k) = e_{vo}(k)
\]

(6)

and, \( \Delta v_m(k) \) is the sampling of the output voltage error \( e_{vo}(k) \).

III. SMALL-SIGNAL MODEL

A precise small-signal model of the control scheme of Fig. 1 is very complex, since it includes analog and digital control variables, synchronous and asynchronous events and variable frequency control update. Instead of very complex models, which handle analog and digital control with variable sampling frequency, a set of approximations has been used in order to provide a simple continuous-time model which represents system dynamics well below half of the switching frequency. More precise and complex models are beyond the scope of this paper.

Linearization of the synchronous/asynchronous modulator is performed using the results obtained in peak current-mode modeling [10]. Among different approaches available in literature [10]-[12], the methodology proposed in [12], where the geometric derivation of the duty-cycle has been derived using waveforms in transient conditions, has been here adopted. Following Fig. 4, the average inductor current over a switching period is then expressed as:

\[
\bar{i}_L = \bar{i}_{pk} - s_f \delta t_{sw} - \frac{1}{2} s_{on} \delta^2 t_{sw} - \frac{1}{2} s_{off} \delta^2 t_{sw}
\]

(7)

where \( \delta = t_{on}/t_{sw} \), \( \delta' = 1 - \delta \), \( s_{on} = v_{in}/L \) and \( s_{off} = (v_o - v_{in})/L \). Large signal averaging (7) has been performed in the analog domain so that its linearized version can be interfaced with conventional time-averaged small-signal model of dc-dc boost converters. Representation of (7) in the discrete domain would require the complex discretization of the dc-dc converter transfer functions under variable sampling times.

Assuming that each variable \( x \) is composed by a steady-state value \( X \) and a small signal perturbation \( \hat{x} \) (i.e. \( x = X + \hat{x} \)), linearization of (7) yields to the following expression:

\[
\hat{\dot{x}} = F_m (\bar{i}_{pk} - \bar{i}_L) + K_f \bar{t}_{sw} + K_{v_o} v_o + K_{v_{in}} v_{in}
\]

(8)

where

\[
F_m = \frac{1}{s_f T_{sw}}
\]

(9.a)
The resulting small-signal model is reported in Fig. 5, where the case when $v_m$ is constant, denoted case A, and the case when $v_m$ is controlled using (3), denoted case B, are shown. In Fig. 5, the separation between continuous-time and discrete-time domain is based on the asynchronous and synchronous contributions, respectively. More precisely, the asynchronous part of the modulator, which imposes switch turn-on and turn-off based on the analog intersections of voltage and current ramps $v_o$ and $i_L(t)$, is reported in the continuous domain. The synchronous part, instead, is reported in the discrete domain, where the derivative action (5) has been represented in the equivalent continuous-time domain.

The validity of (10) and (11) has been verified using time-domain simulations, where a small-signal sinusoidal perturbation has been imposed on the peak current $i_{pk}$ and the output voltage $v_o$. The converter model is quite accurate, with small discrepancies for frequencies approaching 1/4 of the switching frequency. It is worth noting that the modulation of $v_o$ (case B) has a bigger phase shift and thus a slightly less damped response is expected. Even if approximated, we found this model accurate enough for stability analysis and design of regulator coefficients.

For regulator coefficient design and for the derivation of the transfer function seen by regulator regT, (i.e. the transfer function between the peak current $i_{pk}$ and the sampled output voltage $v_{os}$) is simply obtained by sampling transfer function (10) and (11), since in both cases A and B the input of $reg_T$ is a sampled version of the output voltage. In order to account for the sampling process, a simple phase delay of $\pi/2$ has been added to (10) and (11).

As far as the quantization effects are concerned, it worth to point out that the signals $R_{i}(t)$ and $R_{f}(t)$ generated by DACs are quantized. Moreover, the measured switching period of the converter is quantized as well, being an integer multiple of the clock period [9]. However, thanks to the use of the digital current ramp $R_{f}(t)$, the average inductor current can be continuously varied by modulating the delay between the asynchronous switch-on command and the synchronous start of $R_{i}(t)$. As reported in [13], this situation ensures that any state-state load current and voltage can be theoretically supplied without incurring in limit cycles conditions. In order to avoid also the presence of limit cycles enhanced by the digital regulator $reg_T$, the voltage slope $s_{f}$ must be properly designed. More precisely, lower value of voltage slope $s_f$ reduces the possibility of limit cycle oscillations caused by the digital regulator, since the effective resolution in the A/D conversion of the error voltage is increased and the digital controller gain of is reduced. These two conditions increase the immunity of the system from limit cycles, as shown in [3] and [14].
IV. SIMULATION RESULTS

Control algorithm has been initially tested by simulation tools so as to verify the performed theoretical analysis. The converter parameter are: \( V_{in}=24\, \text{V} \), \( V_o=48\, \text{V} \), \( L=28\, \mu\text{H} \), \( C=10\, \mu\text{F} \), \( f_{sw}=200\, \text{kHz} \), \( P_{nominal}=100\, \text{W} \), \( f_{clk}=20\, \text{MHz} \). Coefficient of voltage loop regulator \( \text{regT} \) has been designed so as to ensure a bandwidth of 16 kHz and a phase margin of 60°.

Fig. 7 reports the load step variations (\( R_o = 50\, \Omega \to 25\, \Omega \to 50\, \Omega \) ) for case A. Note that the proposed system gives good dynamic performance with damping and time response which well agree with regulator design. Moreover, the switching period variation is proportional to the output voltage error, as expected by (4). Using the same regulator parameters, we have tested also case B and the results are reported in Fig. 8. Note that in this case the dynamic response is quite similar, but the switching period variation is now the derivative of the output voltage variation, as predicted in (5). A closer comparison between Fig. 7 and 8 is reported in Fig. 9. Note that the frequency modulation is much smaller for case B and the system response has a small overshoot not present in case A. This is also consistent with Fig. 6 due to the higher delay of case B at the crossover frequency.

![Fig. 6 - Verification of the proposed small-signal model (dots 'o' indicate time-domain simulations): case A and B, transfer function between \( i_L \) and \( v_{os} \)](image)

![Fig. 7 - Load step changes (\( R_o = 50\, \Omega \to 25\, \Omega \to 50\, \Omega \) ) with the proposed scheme – Case A.](image)

![Fig. 8 - Load step changes (\( R_o = 50\, \Omega \to 25\, \Omega \to 50\, \Omega \) ) with the proposed scheme – Case B.](image)
V. EXPERIMENTAL RESULTS

For the experimental verification a boost converter has been realized with the following parameters: $V_{in}=24\,V$, $V_o=48\,V$, $L=28\,\mu\text{H}$, $C=10\,\mu\text{F}$, $f_{sw}=200\,\text{kHz}$, $P_{\text{nominal}}=100\,\text{W}$, $f_{\text{clk}}=8\,\text{MHz}$. Two DACs have been used and the digital control has been implemented in an FPGA by Altera, specifically the EP1C20 device, a member of Cyclone family. For the experimental investigation, only case A has been tested.

Fig. 10 reports the dynamic behavior of the digital control under small step changes ($R_o = 75\,\Omega \rightarrow 50\,\Omega \rightarrow 75\,\Omega$). The transient is fast and well damped, without limit cycle oscillations after the load step changes.

For comparison, we have implemented an analog control with peak current-mode control, having a voltage-loop bandwidth of 16 kHz and a switching frequency equal to 200 kHz. Fig. 11 shows the results obtained using the same conditions of Fig. 10. Note that the dynamic behavior is quite similar, showing that the proposed digital solution gives dynamic performance comparable to that of the state-of-the-art of analog controllers at least under small-signal assumptions. Instead, with large-signal step-up load variations we expect our solution to have a slightly higher dynamic response thanks to the frequency modulation. This is also evident by looking at Figure 12 and 13, which report a bigger load step change ($R_o = 75\,\Omega \rightarrow 25\,\Omega$) using the proposed digital control (Fig. 12) and the analog control (Fig. 13). Of course, the opposite properties are expected under large-signal step-down load variations, here not reported due to severe DCM operation.

Finally, it is worth noting that the proposed solution behaves very well in spite of a significant hysteresis band in the two comparators and a large delay in our Mosfet driver (500 ns), as reported in Fig. 14.
VI. CONCLUSIONS

This paper has investigated a mixed synchronous/asynchronous digital controller applied to dc-dc boost converters. It has been shown that the combination of digitally controlled voltage and current ramps and asynchronous switch turn-on and turn-off enable high-dynamic performance while keeping low control complexity. An approximated small-signal model synchronous/asynchronous digital controller has been also derived and used for dynamic performance evaluation. Simulation and experimental results have verified the dynamic performance achievable by the proposed solution for dc-dc boost converters, showing that the overall control performance is comparable to that obtainable with analog peak current-mode control.