Abstract – This paper proposes a digital hysteresis modulation technique based on switching time prediction. Sampling controlled variables several times within a switching period, it ensures a dynamic performance comparable to that obtainable with an analog hysteresis modulation. Compared to conventional digital hysteresis modulation, it avoids frequency jitter since it predicts switching transitions. Compared to hysteresis modulation based on the detection of the zero-crossing of current errors, it avoids external analog circuits. Compared to PWM techniques, it ensures faster dynamic response. These advantages are obtained at the expense of an increased signal processing requirements and of control complexity. Switching frequency stabilization and synchronization with an external clock can be achieved extending the techniques proposed in the past for analog hysteresis modulations. The proposed predictive algorithm does not require knowledge of load parameters and only a rough estimation of the inductor filter, which can be easily self-adjusted. The proposed solution is suited for high-performance current (or sliding-mode) control where the digital hardware has enough computational power to allow multiple samples within a switching period. The proposed modulation technique has been applied to a sliding-mode control of a single-phase Uninterruptible Power Supply (UPS). Experimental results confirm the effectiveness of the proposed approach.

I. INTRODUCTION

The hysteresis current control technique [1-10] has proven to be the most suitable solution for all the applications where control performance requirements are more demanding, since it is characterized by unconditioned stability, very fast response, and good accuracy. The basic hysteresis technique is affected by the drawbacks of a variable switching frequency and of a heavy interference among the phases in the case of a three-phase system with insulated neutral. Effective methods to eliminate these inconveniences have been introduced some time ago and have been demonstrated to be a viable way to obtain robust and high-performance controls [1-9]. Even if the hysteresis technique is essentially an analog one, it has been shown that some parts of its implementation can be done by digital means. For example, in [4] a DSP is used for the control of the bandwidth of an analog hysteresis modulator so as to achieve switching frequency stabilization and synchronization with an external clock. In [5] a technique which can directly modulate the switching leg by digital means is proposed, but it is based on the zero-crossing of the current errors, thus requiring some external analog signal conditioning and control parameters, such as in a sliding-mode control, are still determined by analog components.

Fully-digital hysteresis modulation, which uses only the samples of the controlled variables to determine the switch status, has been widely applied in its basic form, where the modulator switches immediately on and off when the sampled current differs from its reference by a given threshold. This solution, although very simple, has a major drawback due to the frequency jitter associated to the sampling process, which causes spectrum components even in the low frequency range. Indeed, in this digital implementation the turn-on or turn-off times are always multiple of the sampling period, so that unpredictable switching frequency variations are needed to realize the desired average duty-cycle. For this reason, PWM techniques [10,11] are the most commonly used for digital control implementation, even if they offer slower dynamics due to intrinsic modulation delay and current regulator response time.

This paper investigates a digital hysteresis modulation technique based on switching time prediction, which ensures a dynamic performance comparable to that obtainable with an analog hysteresis modulation. The steady-state spectrum is comparable to that of PWM techniques using a simple frequency stabilization algorithm [14]. The proposed solution theoretically avoids frequency jitter associated to conventional digital hysteresis modulation and any external analog circuits, required, for example, by the techniques proposed in [2,4-8], since the modulation is based only on the sampled variables. The proposed approach is suited for high-performance current (or sliding-mode) control and it is motivated by the recent increase of computational power in FPGAs and DSPs, which may allow multiple sampling and calculations within a switching period. The proposed digital control has been applied to the sliding-mode control of an Uninterruptible Power Supply (UPS) using a fixed-point DSP (TMS320F2812). Experimental results on a reduced scale prototype verify the properties of the proposed approach.

II. PROPOSED CONTROL METHOD

The operating principle of the proposed algorithm can be described referring to Figs. 1 and 2, where a standard switching cell with a digital current control is shown. The proposed modulation, here described for the current control of a half-bridge inverter, is equally applicable to dc-dc or ac-dc converters. The description of the proposed control algorithm
is firstly done assuming an ideal operating conditions. Effects of control and switching delays and inverter dead-times are discussed in the next paragraph.

A. Ideal control operation

The algorithm is based on the principle of emulating an analog hysteresis control using only sampled variables and the information on the on (t_on) and off times (t_off) of the previous switching period. Following Fig. 2, the controlled variable \( i_L \) is sampled and compared with a reference \( \text{ref}_L \) each sampling period and, then, depending on the switch status, either the switch turn-off time (\( t_\alpha \)) or the switch turn-on time (\( t_\beta \)) are evaluated and loaded in a up-down counter which determines switching transitions. For the purpose of explanation, we denote S ON when \( v_{inv} = V_{dc} \) and S OFF when \( v_{inv} = -V_{dc} \).

The evaluation of switch turn-on (\( t_\beta \)) when S is OFF and switch turn-off time (\( t_\alpha \)) when S is ON can be calculated at each sampling period using simple geometric considerations on Fig. 2. Using index \( k \) to represent evolutions related to the switching period and index \( h \) to represent sampling instants, we can write

\[
\begin{align*}
  t_\alpha(h) &= \frac{B(k) - \varepsilon_{il}(h)}{p_{on}(k)} & \text{when S on} \\
  t_\beta(h) &= \frac{B(k) + \varepsilon_{il}(h)}{p_{off}(k)} & \text{when S off}
\end{align*}
\]  

where \( p_{on}(k) \) and \( p_{off}(k) \) are the absolute values of the positive and negative slope of the current error during switching period \( k \) and \( \varepsilon_{il}(h) = i_L(h) - i_{ref}^L(h) \). Assuming that the reference current \( i_{ref}^L \) and output voltage \( v_o \) are constant within a switching period, we can write:

\[
\begin{align*}
  p_{on}(k) &= \frac{di_L}{dt} |_{t_{on}(k)} = \frac{V_{dc} - v_o(k)}{L} \\
  p_{off}(k) &= -\frac{di_L}{dt} |_{t_{off}(k)} = \frac{V_{dc} + v_o(k)}{L}
\end{align*}
\]

Solving (2) in steady-state conditions (i.e. \( p_{on}(k) \equiv p_{on}(k-1) \) and \( p_{off}(k) \equiv p_{off}(k-1) \), control law (1) can be written as:

\[
\begin{align*}
  t_\alpha(h) &= G \frac{T_{sw}(k-1)}{t_{off}(k-1)} \left( B(k) - \varepsilon_{il}(h) \right) & \text{when S on} \\
  t_\beta(h) &= G \frac{T_{sw}(k-1)}{t_{on}(k-1)} \left( B(k) + \varepsilon_{il}(h) \right) & \text{when S off}
\end{align*}
\]

where \( G = L/(2V_{dc}) \). Control law (3) is now independent on load voltage \( v_o \) and it is based on the on and off time (\( t_{on}(k-1) \), \( t_{off}(k-1) \)) and the switching period (\( T_{sw}(k-1) \)), evaluated at the previous switching period. These quantities are already available within the controller or can be easily measured with capture and compare units directly connected to the switch signal S.

The proposed switching time prediction (3) is based on time quantities and do not rely on the measurement of the current derivatives for the determination of \( p_{on} \) and \( p_{off} \) slopes, which would have been very difficult to implement. The control law, however, depends on the constant \( G \), which includes converter parameters, possibly time-varying, such as the dc-link voltage. Real-time adaptation of parameter \( G \) is very simple since calculations of switch turn-off (\( t_\alpha \)) and switch turn-on (\( t_\beta \)) time within the same \( t_{on} \) or \( t_{off} \) period are theoretically redundant in steady-state since they differ only by the sampling period \( T_S \). Thus, an integrator on the difference between the different switching time predictions and the sampling time \( T_S \) ensures a simple adaptive law for estimation of parameter \( G \) as long as two samples are available within either the \( t_{on} \) or \( t_{off} \) time.

B. Extension of the operating range

The proposed control described up to now requires at least one sample for every turn-on and turn-off period, imposing a limit in the modulation index. This problem can be easily
overcome calculating at each sampling time \( h \) both the switch turn-off time \( t_{\alpha}(h) \) and the switch turn-on time \( t_{\beta}(h) \). The evaluation of the switch turn-on time \( t_{\beta}(h) \) when \( S \) is ON or the switch turn-off time \( t_{\alpha}(h) \) when \( S \) is OFF is obtained predicting that the current commutates exactly at the hysteresis band. The resulting algorithm is:

\[
\begin{align*}
\text{S ON:} & \quad t_{\alpha}(h) = G \frac{T_{sw}(k-1)}{t_{off}(k-1)} [B(k) - \epsilon_{iL}(h)], \\
\text{S OFF:} & \quad t_{\beta}(h) = t_{\alpha}(h) + G \frac{T_{sw}(k-1)}{t_{on}(k-1)} [B(k) + \epsilon_{iL}(h)],
\end{align*}
\]

where \( t_{\alpha}(h) \) and \( t_{\beta}(h) \) represent the switch turn-off time and the switch turn-on time both evaluated from the sampling instant \( h \).

With this provision the minimum number of samples within a switching period is only one, although higher sampling frequencies are advisable since the proposed technique shows its potentiality when multiple sampling is performed within a switching period.

Algorithm (4) needs to be modified in the case the current error lies outside the hysteresis band so as to ensure the switch status that forces the system variable to go toward the hysteresis band, as in any hysteresis control. Moreover, in the second and fourth equation of (4), the distance between the current error and the hysteresis band needs to be added to the term \( 2B(k) \).

### C. Switching frequency stabilization

As any hysteresis current control, the switching frequency varies depending on load conditions and it can be stabilized changing the hysteresis bandwidth according to the measured switching period. Among different solutions available in literature [4,7,14,15], we have chosen one of the simplest [14], where the bandwidth \( B(k) \) is varied according to the following algorithm:

\[
B(k) = B(k-1) \frac{T_{ref}}{T_{sw}(k-1)}
\]

being \( T_{sw}^{ref} \) the desired switching period. This algorithm ensures switching frequency stabilization after one switching period. Moreover, the synchronization with an external clock can be achieved varying the reference period \( T_{sw}^{ref} \) so as to impose that a specified event (either the turn-on, or the turn-off or the middle of ton period) coincides with synchronization clock.

### III. EFFECTS OF CONTROL NON-IDEALITIES

There are several non-idealities which need to be taken into account in order to evaluate the actual control performance.

Following Fig. 3, the main non-idealities can be summarized as follows: 1) control delays due to A/D conversion and digital implementation (\( T_C \)); 2) delays on switch turn-on and turn-off due to driver circuits and power switch commutation (\( T_D \)); 3) inverter dead-times (\( T_{dead} \)).

#### A. Effects of control and drive delays

The former two points introduce a pure delay on the switch-on and switch-off transitions, causing the actual current to go outside the hysteresis band \( B(k) \), as shown in Fig. 3. This effect causes some errors in (4) and introduces a frequency jitter in the modulation process, even if we found it quite small. Since the delays in the driver stage \( T_D \) and the computational delay \( T_C \) are constant and known (or measurable), they can be easily compensated just leading the actual commutation times \( t_{\alpha}(h) \) and \( t_{\beta}(h) \) by the sum of the two delays. Thus, the actual commutation times become

\[
\begin{align*}
t_{\alpha}^{act}(h) &= t_{\alpha}(h) - T_D - T_C, \\
t_{\beta}^{act}(h) &= t_{\beta}(h) - T_D - T_C.
\end{align*}
\]

where \( t_{\alpha}(h) \) and \( t_{\beta}(h) \) derive from (4). With this compensation, we ensure that the commutation instants occur when the current error is exactly on the hysteresis band, as shown in Fig. 4. In order to avoid an additional error, we need also to skip all samples that occur within a \( T_D \) time after the commutation of the driver signal \( S \), since the control laws (4) assume that the switching has already occurred. An example is reported in Fig. 4, where sample \( h+1 \) is skipped. For the same reason, the sampled variable is skipped if the actual switch turn-off time \( t_{\alpha}^{act}(h) \) or switch turn-on time \( t_{\beta}^{act}(h) \) are negative, so that, for example, in Fig. 4 also sample \( h+2 \) needs to be skipped as well.

#### B. Effects of inverter dead-times

Inverter dead-times introduce two main source of errors. The first is a delay on the switching transition, which depends on
the sign of the current error. The compensation is again obtained by introducing a leading time on the switching transition as follows:

$$t_{\alpha\ominus}(h) = t_{\alpha}(h) - T_D - T_C - (1-K) \cdot T_{\text{dead}}$$

$$t_{\beta\oplus}(h) = t_{\beta}(h) - T_D - T_C - K \cdot T_{\text{dead}}$$

(7)

where $K=1$ when $i_L$ is positive and $K=0$ when $i_L$ is negative.

The second source of error is related to the actual $t_{\text{on}}$ and $t_{\text{off}}$ times used in (4), which are different from those evaluated looking at the driver signal $S$, as reported in Figs. 3-4. The actual $t_{\text{on}}$ and $t_{\text{off}}$ values can be evaluated as:

$$t_{\text{on}}(k) = t_{\text{on}}(k) - \text{sign}(i_L) \cdot T_{\text{dead}}$$

$$t_{\text{off}}(k) = t_{\text{off}}(k) + \text{sign}(i_L) \cdot T_{\text{dead}}$$

(8)

Moreover, the blanking time after switching of the driver signal $S$, mentioned in the previous paragraph, needs to be extended from $T_D$ to $T_D + T_{\text{dead}}$, due to the switching delay introduced by inverter dead-time, as shown in Figs. 3-4.

IV. SIMULATION RESULTS

The proposed algorithm has been initially tested by simulation tools so as to verify the performed theoretical analysis. Due to space constrains, we limit the discussion on the current control of the scheme reported in Fig. 1, where $V_{dc} = 200$V, $L = 3$ mH, and the load is a sinusoidal voltage source with a small amplitude (50V). Fig. 5 reports the behaviour of the proposed technique where the reference switching frequency is 10 kHz and the sampling frequency is 50 kHz. Fig. 6, instead, reports the current spectrum in the case of a sinusoidal current reference with a peak amplitude equal to 10 A. The two figures confirm the excellent dynamic performance, similarly to an hysteresis current control and a good steady-state spectrum. For comparison, we have tested in the same conditions also a conventional digital hysteresis control in its basic form, where the modulator switches immediately on and off when the sampled current differs from its reference by a given threshold. The results are reported in Figs. 7 and 8, highlighting the typical jitter in the commutation instants, which are avoided in the proposed solution.
IV. EXPERIMENTAL RESULTS

The proposed controller has been tested on single phase laboratory prototype based on a full bridge inverter with the following parameters: switching frequency \( f_{sw} \) 10 kHz, dc-link voltage \( V_{dc} \) 200 V, \( L=3.5 \text{ mH} \), \( C=60 \mu \text{F} \). Since the proposed solution is based on a two-level modulation, the full-bridge inverter has been used in the same way, avoiding the application of the zero-voltage level. The extension of the proposed solution to a three-level modulation is under investigation. The digital controller has been developed using a fixed-point DSP by Texas Instruments, namely the TMS320F2812.

We have firstly tested the proposed modulation technique in an inductor current control and results are reported in Fig. 9-11. Fig. 9 reports a step reference variation and clearly shows that the system ensures a dynamic response comparable to that of an hysteresis modulator. The overshoot in the transient response is mainly due to the switching frequency stabilization and due to the erroneous evaluation of the \( t_{on} \) or \( t_{off} \) time in transient conditions. The overshoot is, however, not constant since it strongly depends on the instant of the step variation and the duration of inverter saturation. In Fig. 9 we have reported operating conditions closed to the worst case. Note that, after the step transient, the current presents a smooth and stable behavior. In order to verify the spectral properties of the proposed modulation, we have imposed a sinusoidal current reference and the results are reported in Fig. 10. We can clearly note the switching frequency stabilization and the reduction of the jitter associated to conventional hysteresis current control. Some random variations are, however, still present on our prototype and we have justified them mainly due to the poor signal conditioning on the sensed variables. In order to better understand the conditions of our experimental investigation, Fig. 11 reports the inductor current \( i_L \), which shows our poor signal conditioning, and the sample instants (Sync). Note that one sample is skipped during \( t_{off} \) time, since it would occur just after the switch turn-on time. We have also measured that the driver delay time is 2 \( \mu \text{s} \) and the inverter dead time is 4 \( \mu \text{s} \), which are non-negligible non-idealities compared to the nominal switching period. The control delay due to the DSP has been measured equal to 2 \( \mu \text{s} \).

We have then tested our solution using a sliding-mode control for the UPS prototype. The sliding function \( \psi \) used is the following:

\[
\psi = k_v \left( V_o - V_o^{\text{ref}} \right) + k_i \left( i_C - i_C^{\text{ref}} \right)
\]

(9)

where \( i_C \) is the capacitor current and \( C \cdot k_i/k_v = \tau \) is the first order time constant imposed by the sliding-mode control [12] and designed to be 0.15 ms.

Fig. 12 shows the inverter behaviour with a load composed by a triac and a resistive load. Note the performance is very good, the load transient is recovered very soon. In order to compare the performance of the proposed solution, we have implemented a conventional multi-loop scheme where both the current and the voltage controllers are based on PI regulators. The bandwidth of the current loop was set to 6 \( \text{krad/s} \), with a 60° phase margin, while the bandwidth of the voltage loop was set to 4.5 \( \text{krad/s} \), with a 60° phase margin. An 80% load current feedforward has been included in order to improve the dynamic performance. Fig. 13 shows the results obtained with the same distorting load used for Fig. 12, highlighting the advantages of the proposed solution.

The proposed controller has been then tested in the presence of a distorting load (diode bridge with capacitive filter: 470 \( \mu \text{F} \) filter and 300 \( \Omega \) resistive load). Fig. 14 reports the results of the proposed solution showing that the output voltage waveform exhibits small deviations from the ideal sinusoidal waveform. The performance of the conventional multi-loop PI control with the same distorting load is reported in Fig. 15, confirming the effectiveness of the sliding-mode control in UPS applications.
Fig. 10 – Inductor current spectrum with sinusoidal current reference (vertical scale: 10 dB/div, horizontal scale: 5 kHz/div)

Fig. 11 – Step variation of inductor current reference ($i_L$ - 2A/div, time – 20 µs/div)

Fig. 12 – Proposed solution with triac load: $v_o$ - 40 V/div, $i_o$ - 2 A/div, time - 5ms/div.

Fig. 13 – Conventional multi-loop PI control with triac load: $v_o$ - 40 V/div, $i_o$ - 2 A/div, time - 5ms/div.

Fig. 14 – Proposed solution with diode rectifier load: $v_o$ - 40 V/div, $i_o$ - 2 A/div, time - 2ms/div.

Fig. 15 – Conventional multi-loop PI control with diode rectifier load: $v_o$ - 40 V/div, $i_o$ - 2 A/div, time - 2ms/div.
V. CONCLUSIONS

This paper has investigated a digital hysteresis modulation technique based on switching time prediction. The algorithm is based on the principle of emulating an analog hysteresis control using only sampled variables and the information on the previous turn-on and turn-off time. Using multiple samples within a switching period, it ensures a fast dynamic response, as in any hysteresis control. However, using the switching time prediction, it theoretically avoids the frequency jitter associated to conventional digital hysteresis modulation, ensuring a steady-state spectrum comparable to that of a PWM modulation. It requires, however, increased signal processing requirements due to control complexity. The proposed solution is then suited for high-performance hysteresis-based control where the digital hardware has enough computational power to allow multiple sampling within a switching period. Moreover, due to the provisions and protections needed to cope with the inverter non-idealities, it seems to be better suited for implementation in FPGA, which can easily handle the proposed algorithm with concurrent operations. The proposed modulation technique has been experimentally tested to a sliding–mode control of an Uninterruptible Power Supply (UPS), confirming the theoretical analysis.

ACKNOWLEDGEMENTS

The authors would like to thank Dr. Francesco Cuttini for his support in the experimental activities and Texas Instruments for providing the DSP board.

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