High-Performance Hysteresis Modulation Technique for Active Filters

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Abstract—A new, substantial improvement of the hysteresis current control method for voltage source converters is presented. A simple and fast prediction of the hysteresis band is added to a linearized version of the phase-locked loop control, thus ensuring constant switching frequency and tight control of the position of modulation pulses. This allows high accuracy in tracking highly distorted current waveforms and minimizes the ripple in multiphase systems. The technique implementation is very simple and robust, employing only a small number of conventional inexpensive analog and logic components. It does not require trimmings or tunings, giving the control the capability to adjust itself to the different operating conditions. The proposed method is compared with the most diffused modulation techniques, demonstrating its superior performance in responding to the most demanding conditions met in active filters. The behavior of the method has been fully verified by simulation and by experimental tests.

Index Terms—Active filters, constant switching frequency, hysteresis current control.

I. INTRODUCTION

Converters for active filters must satisfy peculiar requirements regarding the current waveforms and their accuracy. Indeed, in this kind of application, voltage-source current-controlled converters are usually employed, which should produce compensating currents characterized by high harmonic contents and fast transients. Good tracking of the current references has to be ensured, even in presence of nonnegligible harmonics affecting the output line voltage. Moreover, the line and load impedance can be time varying and, within certain limits, unpredictable.

These requirements are much more demanding than those typical of drive applications. Drives are characterized by sinusoidal current waveforms with transients that are comparable with the mechanical time constants. Voltage harmonic contents are limited and, very often, especially in case of induction machines, the sensitivity to current harmonics is limited. Load impedances, even in the case where they are time-dependent, can be estimated with good accuracy.

Thus, for drives, digital current-control techniques are generally employed. The performance of today’s microcontrollers is generally adequate to ensure satisfactory performance with all the advantages typical of the digital approach in terms of reproducibility, ruggedness, flexibility, etc. In particular, the various digital methods (such as the predictive and deadbeat ones) ensure the optimal behavior of the vector control with minimal ripple content and maximum utilization of the dc bus voltage [1]–[4]. Digital controls can be improved if the drive electrical structure can be modeled, thus resulting in a more accurate prediction of the system behavior [5]–[7]. This allows us to minimize the effects of the delays required by A/D conversion and by calculations (one or more modulation cycles), which affects all digital control techniques.

The performance requirements of active filters are hardly met by digital controls slowed down by conversion delays and calculation times. Fast transients and high current-harmonic content call for wide-band controls. To obtain high accuracy and to compensate for the voltage disturbances a high loop gain must be adopted. However, a safe stability margin must be ensured too.

The above requirements conflict with each other. The performance can be improved by increasing the commutation frequency. However, as in active filters, the power involved is quite high and the available switching component do not allow too high frequencies to be adopted. Moreover, as the switching frequency increases, the effects of the dead times increase as well, which add to the voltages disturbances mentioned above.

A satisfactory solution for these requirements has proven to be the hysteresis current-control technique, which is characterized by unconditioned stability, fast response, and good accuracy. Although this technique is essentially an analog one, it has been shown that the major part of its implementation can be done by digital means, thus obtaining several of the advantages typical of digital solutions [8].

The basic hysteresis technique is affected by the drawbacks of a variable switching frequency and of a heavy interference among the phases in the case of a three-phase system with insulated neutral. Effective methods to eliminate these inconveniences have been introduced some time ago and have been demonstrated to be a viable way to obtain robust and high-performance controls [9]–[11]. Additional improvements were proposed [12], [13] to give the system the ability to ensure pulse-phase control to minimize the ripple contents, similarly to the optimal pulse position produced by the vectorial techniques [14].

In this paper, a further and substantial improvement of the hysteresis control is proposed, which is characterized by a very simple and robust implementation. It offers all the advantages of the hysteresis technique. In addition, besides constant switching frequency and phase decoupling, it ensures
a better pulse position control, resulting in the minimization of the ripple. A feedforward/feedback approach, together with linearization techniques, give wide stability margins and self-adjusting capability.

The benefits of the proposed method are demonstrated by comparing the behavior in a typical active filter application with those obtainable by the best implementations of the most diffused digital and analog techniques [4], [15]. Experimental results confirm the advantages of the proposed improvements.

II. PRINCIPLES OF OPERATION

A. Constant Frequency, Hysteresis Current Control

Let us consider first the hysteresis current control of a single-phase voltage-source inverter (VSI) whose an equivalent scheme is shown in Fig. 1. This scheme corresponds quite well to typical active filter application, especially of parallel connection where $L$ and $R$ are the smoothing inductance and its losses and $E$ is the supply voltage.

The instantaneous inverter-output voltage $u$ has a rectangular waveshape of amplitude $\pm E/2$ with a period $T$ and durations of the positive and negative pulses $\tau_p$ and $\tau_n$, respectively (Fig. 2). The load current $i$ satisfies the equation

$$u = R\dot{i} + L\frac{di}{dt} + e. \quad (1)$$

If $i^*$ is the reference current, the instantaneous current error can be defined as

$$\delta = i - i^*. \quad (2)$$

and the reference voltage as

$$u^* = R\dot{i}^* + L\frac{di^*}{dt} + e. \quad (3)$$

From (1)–(3), it results in

$$L\frac{d\delta}{dt} + R\delta = u - u^*. \quad (4)$$

Hysteresis control acts to keep current error $\delta$ within a band of width $\pm\beta / 2$ around zero. Typically, the effects of load resistance $R$ can be neglected, and the reference voltage can be considered constant during a modulation period. Thus, the error $\delta$ has a triangular behavior and the average of the output voltage $u$ over $T$ is equal to $u^*$. By defining the normalized reference voltage

$$u_n = u^*/(E/2) \quad (5)$$

with reference to Fig. 2, it can be derived

$$T = \frac{4\beta L}{E[1 - u_n^2]} \quad \tau_p = T\frac{1 + u_n}{2}, \quad \tau_n = T\frac{1 - u_n}{2} \quad (7)$$

where $\beta$ is the width of the hysteresis band.

If $u_n$ varies and $\beta$ is kept constant, a variable modulation frequency is produced, as shown by (6). To obtain a constant period $T_n$, the hysteresis band $\beta$ should vary in dependence of $u_n$

$$\beta = \frac{ET_n}{4L[1 - u_n^2]} \quad (8)$$

To control $\beta$ for a fixed frequency, a phase-locked loop (PLL) can be used. This solution, adopted in [10], [12] employs the hysteresis comparator as a nonlinear voltage-controlled oscillator (VCO) (Fig. 3, top part only).

When locked to a suitable clock signal, the PLL not only ensures constant modulation frequency, but also minimizes the phase displacement $\phi$ between the output voltage pulses and the clock itself (Fig. 2) with an accuracy limited only by the control loop gain. Indeed, the PLL loop includes a proportional-integral (PI) block (Fig. 3), which integrates the phase displacement and tends to reduce it to zero [8]–[10], [12]. This feature is of particular importance for three-phase insulated neutral systems, where the “centered pulse” condition results in optimal reduction of the current ripple [14].

In controlling the hysteresis modulation, the ability of the PLL to limit the phase displacement is restricted to slow
variations of \( u_n \). This because its bandwidth is limited by the wide variations of the loop gain in dependence of \( u_n \). Indeed, from (6) and (8), the differential gain \( HC \) of the hysteresis comparator turns out to be

\[
HC = \frac{df}{d\beta} = -\frac{E}{4L\beta^2} [1 - u_n^2] = -\frac{f_r}{\beta} \tag{9}
\]

where \( f = 1/T \) is the actual frequency and, in the last term, it is assumed that the system is locked at \( f_r = 1/T_r \).

To reduce the phase displacement and to improve the lock limits, a twofold approach can be used—by modifying the PLL (such as to make the loop gain constant) a wider stability is obtained; besides, a feedforward action is introduced by the prediction of the hysteresis band, thus reducing the PLL error.

The new technique of introducing a variable gain into the PLL loop to compensate for the gain variations of the hysteresis modulator can be implemented by very simple and effective means.

As regards the predictive procedure proposed here, it is free from the parasitic effects and simpler than that proposed in a previous work [12]. Indeed that procedure, even simple, involves analog calculations that call for the use of some operational amplifiers. Moreover, the approximations adopted to simplify that solution introduce, besides the feedforward action, also an unwanted and parasitic feedback signal, which affects the loop gain and the stability. The procedure proposed here is free from that parasitic feedback signal and can be implemented by only an analog switch and few passive components.

### B. PLL Loop-Gain Compensation

A conventional PLL control includes (besides the VCO) a phase detector and a filter, as shown in the top part of Fig. 3 (except the multiplier).

As known, the phase-detector transfer function can be modeled as an integrator

\[
PHD = \frac{d\phi}{df} = \frac{2\pi}{s} \tag{10}
\]

with dimensions \( \phi \) (rad), \( f \) (Hz), and \( s \) (rad/s).

The filter has a proportional integral characteristic to ensure a zero steady-state phase error

\[
PI = \frac{d\beta}{df} = K_p \frac{1 + \tau_s T_z}{sT_z} \tag{11}
\]

with \( K_p \) being the high-frequency gain and \( T_z \) the zero of the filter.

The closed-loop gain \( GP \) in lock conditions is obtained from (8)–(11)

\[
GP = \frac{8\pi K_p L}{E} \frac{f_r^2}{[1 - u_n^2]} \frac{1 + sT_z}{s^2T_z} = -2\pi K_p \frac{1 + sT_z f_r}{s^2T_z} \frac{f_r}{\beta} \tag{12}
\]

The second term of (12) shows that \( GP \) varies with the normalized voltage \( u_n \), becoming very large as its absolute value approaches unity. On the contrary, for small values of \( u_n \) near zero the gain decreases. This behavior is shown in Fig. 4, where asymptotic Bode plots of \( GP \) are reported for \( u_n = 0 \) and \( u_n = 0.8 \).

The large variations of \( GP \) may result in instability. Indeed, to satisfy the stability condition that requires a suitable phase margin at the point where \( GP \) crosses the unity gain, the frequency \( f_z \) of the zero must not be too close to the frequency of the crossing point, even when \( u_n \) is zero maximum and \( GP \) is minimum (Fig. 4). For the same reason, when the gain \( GP \) is maximum, the frequency of the crossing point should be well below (typically a factor of seven) the switching frequency \( f_r \). This is because the commutation process introduces a delay in the control loop, which can be modeled as a pole with a time constant \( T_r = 1/f_r \). The above conditions set a limit both to the maximum loop gain and to the maximum frequency \( f_z \) of the zero.

If these conditions are not met, especially if unity crossing approaches the switching frequency \( f_r \), instability of the PLL may occur. This instability affects the switching regularity and the current error, as illustrated in the example of Fig. 5, where the most significant quantities and in particular the current error \( \delta \) and the positive band limit \(+\beta/2\) are reported versus time. The instability occurs near to the maximum positive and to the minimum negative values of \( u^* \) where \( \beta \) is minimum, according to (8).

To avoid instability, it is customary to set a lower limit to the bandwidth \( \beta \), as explained in [10]. This corresponds to set an upper limit for \( u_n \), beyond which the PLL loses the lock and the modulation frequency slows down.

From the diagram of Fig. 4, it can be seen that to ensure good stability margins and keep the unity-gain crossing well below the switching frequency, the frequency \( f_z \) must be chosen so as to take into account the variations of gain \( GP \) related to the variations of \( u_n \)—the larger the variations, the lower the allowable value of \( f_z \) with respect to the switching
frequency $f_r$. Thus, limited gain and bandwidth of the loop are obtained, which are also variable and reduce appreciably at low values of $t_{th}$.

A solution of this problem is suggested by the expression of $GP$ given by the last term of (12). A constant gain, independent of $\beta$ and, thus, of $t_{th}$, can be obtained if a multiplicative factor proportional to $\beta$ is introduced in the loop, as shown in Fig. 3. This effect, which is usually difficult to implement in analog technique, is easily obtained by taking advantage from the pulsed output of the phase detector.

A possible implementation of this approach is illustrated in Fig. 6. An edge-triggered phase detector is chosen with some simple modifications (such as those described in [16]) that give the alignment of the clock with the center of the modulation pulses, as indicated in Fig. 2. If a detector with three-state output is used (such as the Comparator II included in the IC CD4046) it ensures the widest capture range. The comparator produces positive or negative pulses according to the sign of phase error $\phi$ and of duration proportional to its value. By using these pulses to drive two analog switches fed by voltages $+V_\beta$ and $-V_\beta$ proportional to $\beta$, a series of pulses is obtained at the input of the PI filter, which have a short-term average value proportional to $\phi \cdot \beta$. Expression (12) of the loop gain becomes

$$GP^* = -2\pi K_\beta \frac{1 + sT_z}{s^2T_z^2} f_r K_\beta$$

(13)

where $K_\beta$ is a proper constant. As a result, $GP^*$ is independent of $t_{th}$. In this case, a better choice of the PI filter parameters is allowed for the same phase margins and unity gain crossing, as shown in Fig. 4. In particular, as the gain does no longer vary, a high value $f_{z}^*$ of the zero frequency can be adopted. Thus, a wider control bandwidth and especially higher gains at high frequencies are obtained, which do not depend on $t_{th}$.

In practice, if the PLL control is acting alone, only the bandwidth value $\beta_2$ at the output of the PI filter can be used for the multiplication. This determines a minor closed loop, which introduces some changes in the overall loop gain. However, as phase error $\phi$ is kept small, this effect can be neglected. Instead, if a prediction of the bandwidth is also adopted (as described in the next section), the estimated value $\beta_2$ can be used (Fig. 3). In this case, no parasitic loops are introduced and the loop gain is given by (13).

C. Prediction of the Hysteresis Band

To calculate the hysteresis bandwidth $\beta_2$, which produces the desired switching frequency $f_r$ with a given value of $t_{th}$, a comparison should be made between (6) and (8). Starting from the actual frequency value $f$ and from the corresponding period $T$, the bandwidth $\beta_2$ is exactly derived from the actual bandwidth [13] according to

$$\beta_2 = \beta \frac{T}{T} = \beta \frac{f}{f_r} = \frac{\beta kT_r}{T}$$

(14)

A very simple analog implementation of (14) is sketched in Fig. 7. Every switching period $T$, the switch $SE$ is closed for a time $kT_r$, thus applying voltage $\beta f/k$ to the input of the low-pass filter. A series of pulses is produced whose average value is $\beta_2$, according to (14), irrespective of the actual value of $T$. A suitable value of $k$ less than one (e.g., 0.5), must be chosen to ensure proper operation even when the actual switching frequency $f$ exceeds $f_r$.

This calculation method gives the correct value of $\beta_2$ within one period delay. However, a further delay is introduced by the filter to smooth the signal enough to ensure a proper operation of the hysteresis comparator. The timing of the switch can be given by a monostable multivibrator (MMV) triggered by a commutation pulse edge. Of course, to avoid any adjustment, it is an easy task to obtain the switch timing from the same clock which produces the reference $f_r$.

The predictive method proposed is so effective that it can be used alone (as in [11]) in case only the commutation frequency is of concern, but not the phase error. If this latter must be kept under control, the PLL action is also needed.

D. Feedforward/Feedback Modulation Frequency Control

The predicted bandwidth $\beta_2$ may be added to the term $\beta_1$ resulting from the PLL control, giving a feedforward/feedback compensated gain control of the modulation frequency according to Fig. 3. In theory, if the value of $\beta_2$ was the exact one, the PLL output $\beta_1$ should be zero. In practice, $\beta_2$ is reduced to the small amount needed to correct for the inaccuracies and the delays of the prediction of $\beta_2$, as shown in Fig. 8. Correspondingly, the phase error $\phi$ required by the PLL is reduced too, thus resulting in a better performance and/or in a less critical setting of the control.

It should be pointed out that as the predictive method is truly a feedforward one, no parasitic loops are introduced (see, for comparison, [12]). Thus, the PLL stability can be analyzed as it was acting alone.

The improvement of the feedforward/feedback control in reducing the phase displacement may be evaluated by reference with the phase errors obtained by a hysteresis control with sinusoidal current and voltage outputs of frequency ranging
from 50 to 150 Hz and for various modulation indexes \( m \) (\( m = u_m \) at the peak of the output voltage). First, the behavior with a conventional PLL was simulated with and without a feedforward predictor (Fig. 9). Second, simulated phase errors, given by a PLL (gain-compensated as proposed above), with and without feedforward prediction, are reported in Fig. 10. Both controls were set at the same safe stability margin.

The comparison of the two diagrams allows to evaluate the significant benefits both of the gain compensation and of the feedforward action.

### III. MULTIPHASE CONVERTERS

In multiphase converters with a noninsulated neutral wire, every phase operates independently from the others and the preceding considerations can be applied separately for each of them. Instead, in insulated neutral (or delta connected) multiphase systems or in single-phase bridge converters with nonsynchronous legs (such as in [16]), there is interference among phase commutations and hysteresis control operation can be severely affected [15]. However, it has been shown and repeatedly illustrated in previous papers that completely interference free operation is obtained in case of symmetric load if the hysteresis control of each phase is performed instead of the true current error \( \delta \) defined by (2) on a modified error

\[
\delta' = \delta - \delta''
\]

where the correcting term \( \delta'' \), common to all phases, is defined by

\[
\delta'' = \frac{u_0}{sL + R}
\]

\[
u_0 = \frac{m_1 + m_2 + \ldots + m_n}{n}
\]

being \( n \) the number of phases and \( u_0 \) the load midpoint instantaneous voltage [10]–[13], [16]. According to (16), the calculation of \( \delta'' \) is a simple task, easily performed by means of analog techniques, once known as the load parameters \( L \) and \( R \). For decoupling purposes, the calculation is not critical: typically for \( L \) an approximated estimation is sufficient and the influence of \( R \) can be neglected.

With the above approach, the proposed improved hysteresis control method can be extended to the large majority of applications.

### IV. HYSTERESIS CONTROL OF THE ACTIVE FILTERS

In active filter applications, the inverter is used to correct for the harmonics and distortions produced by the load [17]–[20]. In case of shunt active filters [17], [20], the load current distortion is compensated by the inverter current according to a general scheme like that of Fig. 16. The inverter behaves as a current source controlled by a reference signal, which corresponds to the difference between the current waveform wanted for \( i_S \) at the supply side and the actual load current \( i_L \). At this purpose, every kind of inverter capable of current control can be used. The trend is today toward the voltage-source current-controlled inverters, using one of the many analog or digital current control techniques available.

In shunt-connected active filters (Fig. 16), the line voltage acts as electromotive force (EMF) \( e \) of Fig. 1. Thus, the inverter has to deliver a voltage with a large amount of first harmonics, plus a fraction mainly due to the voltage drop caused by the current on the smoothing inductor \( L \), which is rich of harmonics and pulses corresponding to the transients. This is a challenging requirement for every current control.

In particular, in the hysteresis controls, as the hysteresis band must vary with the delivered voltage to maintain a fixed
switching frequency, a wide bandwidth of the PLL loop is needed to follow the voltage transients with good accuracy. However, as discussed in the previous sections, the PLL bandwidth is limited by the switching frequency, which, in high-power applications, cannot exceed a few kilohertz, even with insulated gate bipolar transistor (IGBT) inverters.

The behavior of a three-phase inverter with the proposed feedforward/feedback hysteresis control and acting as an active filter was simulated under a variety of conditions and compared with that of different control techniques.

In Figs. 11–15, the simulation results are shown for the case of a shunt-active filter compensating a rectifier load (Fig. 16). This is a typical application of active filters with load current including high-order harmonics and steep transients.

To illustrate the improvements of the proposed control, operating conditions are chosen at the limits of its tracking capability.

A low switching frequency $f_\text{r} = 5 \text{ kHz}$ is adopted, typical of large power converters. To ensure wide stability margins, the control parameters turn out to be PLL zero frequency $f_\Sigma = 1/2\pi T_\Sigma = 540 \text{ Hz}$, PLL filter gain $K_\Sigma = 0.42$, $K_\beta = 0.5$, feedforward filter bandwidth $f_e = 1/2T_e = 790 \text{ Hz}$. Thus, a significant gain of the PLL loop and of the feedforward action is ensured only for the harmonics of order below the 11th. This means that with the kind of load considered, the control ability to follow the output voltage variations and to maintain a constant switching frequency is hardly sufficient.

The other converter and load parameters are the same adopted in experimental tests.

In Fig. 11, the load current $i_L$, the converter current $i_c$ and its reference $i^*$, the resulting supply line current $i_S$ and its reference $i_S^*$, and the calculated converter reference voltage $u^*$ are given for one phase.

As shown in Fig. 11, a limited rate of rise and fall of the load current $i_L$ is assumed to keep the voltage $u$ within the boundaries of the converter supply voltage. This prevents the saturation of the current control, thus ensuring a full compensation of the load current harmonics.

In Fig. 12 (in more detail), the converter total current error $\delta$ and pulse phase error $\phi$ are shown together with $i_S$ and $i_S^*$ for reference.

It is usual to evaluate the error of a current control in terms of rms value of the current ripple. Although this figure is more...
suitable to express the disturbances created in a drive than in an active filter, it can be used even in this case. For the error of Fig. 12, the rms ripple results to be 0.38 A rms.

In Fig. 13, $i_S$, $\delta$, and $\phi$, obtained by a hysteresis current control using a conventional PLL [10], are reported for comparison. To ensure stability, the control bandwidth of the PLL has to be fixed about ten times lower than that of the compensated PLL.

As can be seen, the phase displacements with the conventional PLL are much worse than those given by the proposed control. These latter, however, in the conditions chosen for the simulation, are by no means negligible, owing to the bandwidth limitations said above. It should be put in evidence that both controls are able to follow the reference current without converter saturation once ensured a suitable margin of the supply voltage. The performance difference consists in the ability to maintain a constant switching frequency and to limit the phase displacements.

Simulation results show also that a more regular hysteresis band and a reduced ripple amplitude are obtained with the proposed control (the ripple in Fig. 13 is 0.54 A rms). The improvement is related to the bandwidth increment, although limited, and to the feedforward action which allow better stability margins. These benefits are even more important that that of the phase-error reduction.

The line currents and current errors given by classic ramp comparison (i.e., sine triangle) [15] and by digital deadbeat [4] current controls (in the same conditions as above) are shown in Figs. 14 and 15. For these techniques, the phase error $\phi$ is intrinsically controlled and exactly kept to zero in deadbeat control. As regards the current errors, however, both methods exhibit appreciable deviations in correspondence with the edges of the load current, which impair the accuracy of the compensation. Despite the big current peaks, the differences with the previous controls look less appreciable if evaluated with respect to the rms current error, which results to be 0.74 A rms for the ramp comparison and 0.86 A rms for the deadbeat.

It should be mentioned that the deadbeat method simulated also requires, in addition to current sensing, picking up the supply-line voltages.

The simulations performed demonstrated that even larger advantages would result from the proposed method in the case of current steps that saturate the converter voltage so that the current control loop loses control. In this instance, only the hysteresis techniques ensure fast recovery while the other methods exhibit longer and wider transients.

V. EXPERIMENTAL TESTS

The hysteresis current control implemented according to the above proposal was applied to a three-phase voltage source converter acting as a shunt-connected active filter (Fig. 16).

The experimental set was intended as a reduced scale model of large-power applications. Thus, a modulation frequency $f_r = 5$ kHz was chosen. Consequently, to keep the modulation ripple within reasonable limits, smoothing inductors of $L = 12.5$ mH, $R = 2.2$ Ohm were used with a dc bus voltage $E = 800$ V.

The load to be compensated was a full bridge three-phase uncontrolled rectifier fed by a 380-V rms line-to-line voltage, delivering 512 V and 11 A to a compound excited dc motor.

Inductors of value $L_L = 1$ mH were inserted at the rectifier input, to limit the rate of rise and fall of the load current at the commutations of the bridge. This ensures a full compensation capability of the filter, as explained in the previous section. The effects of these inductances corresponds to that given, in many cases, by the leakage inductance of the transformer feeding the rectifier.

Filter capacitors of value $C_1 = 3 \mu$F for the modulation ripple were put in parallel to the supply line, together with damping units made up by resistors $R_2 = 15$ Ohm and capacitors $C_2 = 10 \mu$F. The supply-line inductance was estimated to be 0.9 mH.

The values assumed for the control parameters were the same of the simulation: PLL zero frequency $f_z = 1/2\pi T_z = 540$ Hz, PLL filter gain $K_p = 0.42, K = 0.5$, feedforward filter bandwidth $f_c = 1/2\pi T_c = 790$ Hz.

The system behavior was extensively tested, both in transient and steady-state conditions at different values of the current drawn by the motor.

The hysteresis control demonstrated to be stable, with fast response and accurate harmonic compensation for the whole operating range. In particular, more robustness was achieved against line-voltage fluctuations and imbalances with respect to classic PLL hysteresis control. This improvement may be attributed to the feedforward action and to the large stability margins that could be adopted for the PLL loop without impairing the compensation accuracy.

As an example of the performance of the experimental prototype, in Fig. 17 the phase-supply voltage $v_{SS}$ and current $i_S$, resulting from the filter compensation are shown together with the rectifier input current $i_L$. This latter, as the supply voltage remains practically unchanged, is identical to that entering the rectifier before the filter is operated.
to allow not only constant frequency operation even for rapid rates of changing of the output voltage, but also improved control of the position of the modulation pulses. This latter feature is of particular importance in reducing the current ripple in insulated neutral multiphase systems where the optimal reciprocal position of the modulation pulses of the phases is the “centered” one.

A substantially wider bandwidth and better stability of the PLL controlling the frequency are achieved by means of a compensation of the variation of the loop gain with the output voltage and by adding a prediction of the correct width of the hysteresis band. The prediction method is much simpler and more effective than that proposed in a previous paper [12]. Hysteresis control operation requires to sense only the output currents and needs no adjustments or trimmings.

The performance of the proposed method has been compared with those of the most popular modulation techniques. It was demonstrated the superior ability of the hysteresis method to follow with small error the most distorted current waveforms met in high-demanding applications such as the active filters.

The method has been studied in detail by means of theoretical analysis and simulation. Extensive experimental tests on a prototype confirmed the effectiveness of the improvements proposed and the robustness of the resulting control.

VI. CONCLUSIONS

Substantial improvements are proposed to the hysteresis current-control technique for voltage source inverters, intended

The good compensation ensured by the active filter, even with a quite distorted load current, is demonstrated by the resulting input current waveform.

In Fig. 18, the compensating filter current is shown for one phase together with the for reference. The absence of oscillations even in correspondence of the steep transitions of the current demonstrates the stability of the control operation.

In Fig. 19, the corresponding total converter error δ is reported, again referenced to the phase current. The good correspondence with the simulated behavior of Figs. 11 and 12, in particular, at the current transitions, can be appreciated. The good response of the control is confirmed by the regularity of the error signal δ.

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IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 12, NO. 5, SEPTEMBER 1997


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